bc350VME
Time Code Reader/Generator

User's Guide

CHAPTER ONE
INTRODUCTION

1.0 GENERAL

The bc350VME VMEbus Time Code Processor Operation and Technical Manual provides the following information:

- General Introductions.
- Installation and Setup Details.
- Operation and Software Interface Details.
- I/O Theory of Operation.
- Drawing Set.

1.1 bc350VME FEATURES

The bc350VME VMEbus Time Code Processor Operation offers the following features:

- Decodes the commonly used time code format IRIGB.
- Continues to provide time during loss of input references.
- Provides the 0.5 microsecond resolution.
- Allows time capture via an external event trigger input.
- Outputs IRIG-B time code locked to the IRIGB input.
- Output IRIG-B flywheels if input signal is lost.
- Functions as an A16:D08(O) slave with flexible interrupt capabilities.
- 4K byte lock can be located on any 4K byte boundary in the VMEbus short address space.
- Provides both front panel and P2 I/O connections.
- Drives LED display with the decoded IRIG B time, (hours, minutes, seconds).
- Outputs 10MHz and 1PPS disciplined to the IRIG B time code.

1.2 bc350VME OVERVIEW

The bc350VME is a double height (6U) module designed to decode serial IRIG-B time code signals for time tagging in date acquisition applications.

The operation of the bc350VME is controlled by registers written and read by the host via VMEbus A16:D8(O) data transfers. These registers are used for:

- Defining the modes of operation.
- Activating time capture operations.
- Holding the captured time and status.
- Defining on-board interrupt priority levels and vectors.

The principal performance characteristics are listed in Table 1-1 on the following page.

Table 1-1
bc350VME Performance Specifications

Item	Description
Time Code Reader	
Time Code Format	IRIG-B
Carrier Range	1kHz +/- 2%
Flywheel Accuracy	Drift <2ms per hour
Modulation Ratio	3:1 to 6:1
Input Amplitude	0.5V to 6V peak-to-peak
Input Impedance	5KΩ (AC coupled)
VMEbus Interface	
Standardization	Revision C.1 of the VMEbus Spec
Address Space	A16, AM Codes $29 and $2D
	4K Contiguous bytes
Data Transfer	D08 (O)
Interrupter	D08 (O), I(1-7), ROAK
Power	+5VDC @ 1.1 A
	+/- 12VDC @30mA
TTL/CMOS Input Signals	
Event Capture	TTL/CMOS, Positive or Negative Edge Triggered, 50 ns min width, 500µs min period
TTL/CMOS Output Signals	
1 Pulse Per Second	TTL/CMOS, Positive edge on time

CHAPTER TWO
INSTALLATION AND SETUP

2.0 GENERAL

The bc350VME is a double height (6U) VMEbus board designed to be installed in a standard VMEbus subrack. This section details the steps required to install the module in the subrack.

2.1 BASE ADDRESS SELECTION

Before installing the module in the subrack, the four position address select DIP switch (SW1) must be set. The bc350VME occupies 4K bytes in the VMEbus short address space and can be freely located on any 4K bytes boundary. The 4DIP switch positions of SW1 correspond to the address bits A15 - A12 as shown in Figure 2-1 and determine the base address for the module. The base address is defined as the address selected by the SW1 DIP switch when All - A1 are 0.

DIP Switch SW1

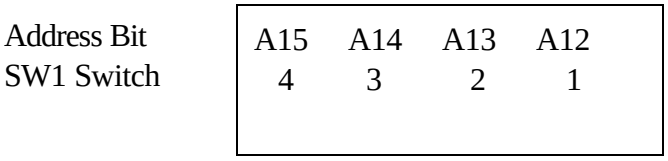


Figure 2-1: DIP Switch SW1

To select a base address, set each of the 4 DIP switches to the ON (same as CLOSED) or OFF (same as OPEN) position. Setting a DIP switch to the ON position selects a logical “0” for that address bit, and the OFF position selects a logical “1”.

The bc350VME responds to address modifiers $2D (Short Supervisory Access) and $29 (Short Non-Privileged Access) as decoded by address modifier decoder PL U34. This decoder PLD can be modified by the factory to decode different and/or additional address modifiers. Consult the factory for custom address modifier decoding.

2.2 INSTALLATION PROCEDURE

Once the base address has been selected, the bc350VME is ready to be installed in the VMEbus subrack. Install the bc350VME as follows:

- Remove IACKIN*/IACKOUT* backplane jumper for the bc350VME slot. This step should be done even if you will not be using interrupts for the bc350VME.

- Verify that the power to the subrack is turned off before inserting the bc350VME module into the subrack.

- Insert the bc350VME into the subrack slot and secure the board in this slot by tightening the 2 front panel screws.

2.3 JUMPER SELECTIONS (see Schematic Diagram 11520-A)

Group JP4 JP6 JP9

JP4 open (not used factory diagnostic)
JP6 jump (GPS serial data input) (bc700VME only)
JP9 open (not used future expansion)

Group JP3 JP5 JP8

Normal Operation

JP3 open
JP5 jump
JP8 jump

Generator Diagnostic

JP3 jump
JP5 open
JP8 open

Host Diagnostic

JP3 open
JP5 jump
JP8 jump

Group JP2 JP7

Modulated Time Code Output

JP7 jump
JP2 open

DC Level Shift Code Output

JP7 open
JP2 jump

CHAPTER THREE

OPERATION AND SOFTWARE INTERFACE

3.0 GENERAL

The bc350VME occupies 4K bytes in the VMEbus short address space (2K D08 "O" memory locations). Refer to Section 2.1 for details on base address selection. All data transfers between the VMEbus and the bc250VME are D08 "O" type (single odd byte transfers). This chapter describes the bc350VME memory locations and their use.

3.1 CONTROL AND TIME TRANSFER

This section describes the locations used on the bc350VME for controlling its operation and transferring time data. The memory map of the bc350VME is listed in Tables 3-1 through 3-3. The first column of these tables shows the offset from the base address of each register. The value of each location following a VMEbus SYSRESET* is shown where '- - ' indicates that the location content is undefined. A label for each location is listed as a brief identifier of the location's function.

Table 3-1
Control Locations

Offset (Hex)	Reset Value	Label	Description
001	00*	TCSEL	Time Code Format Select
003	00	DVINTEN	Data Valid Int Enable
005	00 *	EVENT	External Event Control
007	01 *	MODE	Mode Control

* = warmstart required to change the value

TCSEL - Not currently implemented, unit decodes only IRIGB.

DVINTEN - Data Value Interrupt Enable

Bit 0: 0 = no interrupt on requested time ready
1 = interrupt on requested time ready
Bit 1: 0 = no interrupt on event capture time ready
1 = interrupt on event capture time ready

EVENT - External Event Edge Control (J1-3 pr P2-C6)

0 = event capture disabled
1 = event capture on falling edge of input
2 = event capture on rising edge of input
3 = event capture on both edges of input

Table 3-2
bc350VME Memory Map

Offset (Hex)	Reset Value	Label	Description
043-05D	--	REQTIME	Requested Time Data Block
023-03D	--	EVTIME	Ext Event Time Data Block
041	--	STATO	Status Byte
621-631	--	SETIME	Input Major Time Data
7FD	01	CMD	Command
7FF	--	INT3ACK	Int Source 3 Acknowledge
C01	--	TIMEREQ	Time Request
A01	--	STAT1	Read Stat / Clear Stat
A03	--	STAT2	Clear Stat
801	00	INTCR0	INT Control Register 0
803	00	INTCR1	INT Control Register 1
805	00	INTCR2	INT Control Register 2
807	00	INTCR3	INT Control Register 3
809	0F	INTV0	INT Vector Register 0
80B	0F	INTV1	INT Vector Register 1
80D	0F	INTV2	INT Vector Register 2
80F	0F	INTV3	INT Vector Register 3
E01	--	PINTCLR0	Pending Interrupt Clear 0
E03	--	PINTCLR1	Pending Interrupt Clear 1
E05	--	PINTCLR2	Pending Interrupt Clear 2
E07	--	PINTCLR3	Pending Interrupt Clear 3

Table 3-3
Time Data Blocks Format

Offset (Hex) Event/Req	Data (ASCII Digits)
023/043	Days Hundreds
025/045	Days Tens
027/047	Days Units
029/049	Hours Tens
02B/04B	Hours Units
02D/04D	Minutes Tens
02F/04F	Minutes Units
031/051	Seconds Tens
033/053	Seconds Units
035/055	Subsecond Count Byte 0 (MSB)
037/057	Subsecond Count Byte 1
039/059	Subsecond Count Byte 2
03B/05B	Frequency Offset MSB
03D/05D	Frequency Offset LSB

3.1 CONTROL AND TIME TRANSFER (continued)

MODE - Operating Mode Control

0 = Use IRIGB Timecode for time reference.

2 = Use event input for one second epoch reference. Set major time via the SETGEN command.

3.1.1 REQUESTING CURRENT TIME

The current time may be requested by writing to offset location C01H. A write to this location produces an interrupt and causes the current time to be latched. The interrupt processing routine transfers the latched data to the offset locations indicated in Table 3-2. When the data is ready (typically 200 usec) bit 0 of offset location A01H will be set. It is the responsibility of the host VME processor to clear this bit by writing any value to offset A01H. It is recommended that this be done just prior to the time request. INT3 may be enabled via control location DVINTEN to signal the availability of the requested time data. The 200 µsec delay between the time request and time data availability is only a latency issue. The time is frozen at the instant that the Time Request Register is accessed.

3.1.2 LOGGING HARDWARE EVENT TIMES

A rising (TTL or CMOS) edge at J1-3 or P2-C6 will interrupt the bc350 CPU in a manner similar to a write to offset C01H as described above. Time will be latched and a service routine will transfer both major and minor time data to the locations specified in Table 3-3. When the time data is ready, bit 1 of offset A03H will be set. The host VME processor is responsible for clearing this bit by writing any value to offset A03H. INT3 may be enabled via control location DVINTEN to signal that an event has been detected. The event input is programmable for either positive or negative edges on both, via control location EVENT.

3.1.3 USING SUBSECOND COUNT DATA AND FREQUENCY ERROR DATA

The minor time (less than integer second) associated with the requested time and the event time is in a straight binary format with a resolution in 0.5 µsec. Therefore, 21 bits of data are needed to specify the number of 0.5 µsec in the minor time. The most significant byte, subsecond count byte 0, contains 5 bits. And subsecond count bytes 1 and 2 each, contain 8 bits. The subsecond data is obtained from a free running counter driven by a 2 MHz crystal oscillator. The counter is set to zero synchronously with the time reference one second epoch. The 2 MHz oscillator may not be perfect. For example, a frequency offset of 5 parts per million would result in a minor time error of up to 10 binary counts near the end of a one second epoch. For this reason the value of the least significant 16 bits of the minor time set at the end of a one second epoch is maintained in the frequency offset byte locations. If the 2 MHz oscillator were perfect, then these bytes would contain the decimal value 33920. A value higher than 33920 indicates that the 2 MHz oscillator is fast, and a value less than 33920 indicates that the oscillator is slow. The minor time may be scaled as follows.

(minor time) = (minor time) * 2E6 / (2E6 + (freq error - 33920))

The difference between minor time and scaled minor time is very small, usually on the order of a few parts per million.

3.1.4 STATUS BYTE 0 (OFFSET 041H)

The value of this byte is a function of bc350 mode. When operating in mode 0 (reading timecode) STATO will have a value of “0” or “1”. A value of zero indicates that time is being decoded properly. A value of one indicates that time is not being decoded and that the bc350 is ‘flywheeling.’

3.1.5 COMMAND BYTE (OFFSET 7FDH)

The command byte has been allocated to a unique position in the bc350 address space. A write to this location by the VMEbus host processor drives a special purpose output line low on the dual port ram. This line is connected to an interrupt input line on the bc350 supervisor CPU. A command byte write will generate a high priority interrupt. The value of the command byte is used by the interrupt processing routine to determine what action is to be taken. The following command bytes are currently implemented.

Value	Pneumonic	Action
1	WARMSTART	Reset (no variable initialization)
3	EVLOAD	Load event control value
4	TOGGLE	Factory test toggles (do not use)
5	TOGGLE	Toggle diagnostic messages
6	TOGGLE	Toggle disciplining
7	TOGGLE	Factory test toggle (do not use)
8	JAMSYNC	Enable LCA jamsynch to reference
9	RESET	Same as power on reset
10	BCOMF	Generate special BCOMF timecode
16	SETGEN	Set generator time

3.1.5.1 WARMSTART

The warmstart command is used whenever it is desired to change an operating parameter from the power on default value. Currently only the four parameters in Table 3-1 are in this category. The EVENT control location can also be changed with command value 03 (EVELOAD).

3.1.5.2 TOGGLES

All the toggle commands simply ‘toggle’ a function on or off and are used primarily during diagnostic testing. The use of the toggle commands is not recommended.

3.1.5.3 JAMSYNC

The JAMSYNC command causes the disciplined 1 PPS to be 'jammed' into synchronism with the reference 1 PPS (either timecode or external). This command is most useful when switching from one reference to another. The disciplined oscillator phase lock loop has a closed loop bandwidth on the order of millihertz, and it would take a few minutes to stabilize to a new one second epoch that was only milliseconds different from the previous reference.

3.1.5.4 RESET

The reset command causes the bc350 host processor to begin execution at the power on reset code entry point.

3.1.5.5 BCOMF

BCOMF is an acronym for Datum-F timecode. This is a special purpose timecode with built-in error protection used in applications where it is desirable to never display an incorrect time. It may only be used with equipment specifically designed to decode it. This command causes the generator to generate the BCOMF time code.

3.1.5.6 SETGEN

This command sets the time code generator with the time values that have been previously stored at the following offsets.

seconds units	ASCII	621H
seconds tens	ASCII	623H
minutes units	ASCII	625H
minutes tens	ASCII	627H
hours minutes	ASCII	629H
hours tens	ASCII	62BH
days units	ASCII	62DH
days tens	ASCII	62FH
days hundreds	ASCII	631H

When the bc350 is decoding time code, the generator is automatically set to the decoded time. Therefore, the generator time can be set only in the absence of time code or when using operating mode 2 (MODE = 2).

3.2 INTERRUPT CONTROL, VECTOR AND PINTCLR REGISTERS

The bc350VME supports four independent interrupt sources (interrupt source 0-3). Associated with each interrupt source are three registers:

- one Interrupt Control Register.
- one Interrupt Vector Register.
- one Pending Interrupt Register.

3.2.1 Interrupt Control Registers

The Interrupt Control Registers govern the operation of the VMEbus interrupts. There is one control register for each interrupt source. For example, INTCRO controls interrupt source 0, INTCR1 controls interrupt source 1, etc. The Interrupt Control Register format is shown below.

Bit	7	6	5	4	3	2	1	0
Function	FLAG	FAC	X/IN	IRE	IRAC	L2	L1	L0

L2, L1, L0 = Interrupt Level. The Three interrupt level bits determine the level at which an interrupt will be generated.

L2	L1	L0	IRQ LEVEL
0	0	0	DISABLED
0	0	1	IRQ1
0	1	0	IRQ2
0	1	1	IRQ3
1	0	0	IRQ4
1	0	1	IRQ5
1	1	0	IRQ6
1	1	1	IRQ7

IRAC = Interrupt Auto Clear. If the IRAC is set, IRE (Bit 4) is cleared during an interrupt acknowledge cycle responding to this request. This action of clearing the IRE disables the interrupt request. To re-enable the interrupt associated with this register, IRE must be set again by writing to the control register.

IRE = Interrupt Enable. This bit must be set to "1" to enable the bus interrupt request associated with the control register.

X/IN = External/Internal Vector. This bit must be cleared in all cases.

FAC = Flag Auto Clear. If FAC is set to 1, the FLAG bit is automatically cleared during an interrupt acknowledge cycle.

FLAG = Flag Bit. This bit is a flag that can be used for processor-to-processor communication, and resource allocation. The FLAG bit has no affect on the operation of the interrupts.

3.2.2 INTERRUPT VECTOR REGISTERS

Each of the four interrupt sources has associated with it an interrupt vector register. Interrupt source 0 uses INTV0, interrupt source 1 uses INTV1, etc. The 8 bit interrupt vector is supplied to the VMEbus during an interrupt acknowledge cycle. The four Interrupt Vector Registers are set to 0F at reset which corresponds to the MC68000 vector for an uninitialized interrupt vector.

3.2.3 PENDING INTERRUPT CLEAR REGISTERS

Associated with each of the four interrupt sources is a Pending Interrupt Clear Register. Interrupt source 0 uses PINTCLR0, interrupt source 1 uses PINTCLR1, etc. These registers are used to clear any pending interrupt signals before interrupts are enabled with the Interrupt Control Registers. A pending interrupt is cleared by reading or writing any value to the appropriate Pending Interrupt Clear Register. Before enabling interrupts with INTERCX, the user should clear any pending interrupts associated with interrupt source X.

3.2.4 INTERRUPT SOURCE 3 ACKNOWLEDGE REGISTER

Interrupt Source 3 requires an acknowledge operation following the interrupt. Before another interrupt from Source 3 can take place, the Interrupt Source 3 Acknowledge Register must be read. The contents of this register are meaningless. Interrupt sources 0-2 do not have corresponding interrupt acknowledge registers.

3.3 TIME CODE GENERATION

IRIGB timecode is generated at J2 on the front panel. The timecode is synchronized to either the IRIGB timecode read in mode 0 or the external 1PPS input in mode 2. An amplitude adjust potentiometer, VR1, is located below the J2 output BNC.

3.4 VMEbus INTERRUPTS

The bc350VME provides 4 independent VMEbus interrupt sources as shown in Table 3-4. As described above, associated with each interrupt source are three registers:

- an Interrupt Control Register.
- a Vector Register.
- a Pending Interrupt Clear Register.

Each interrupt source can generate an interrupt on any one of the seven interrupt request levels (IRQL) on the VMEbus. All four sources could also use the same IRQL. Additionally, each interrupt source can have its own unique interrupt vector. The following sections describe the operation of each interrupt source.

Table 3-4
bc350VME Interrupt Sources

INT Source	Function
0	1 Pulse Per Second
1	Future Implementation
*2	Heartbeat Pulses
3	External Event/Time Request Time Valid

* = not implemented

3.4.1 INTERRUPT SOURCE 0 (1 PULSE PER SECOND)

The bc350VME generates a 1 Pulse Per Second (1PPS) signal. This signal generates a rising edge which occurs at the on time mark of the time code signal, and is available on the J3 I/O connector. This 1PPS signal can also be used to generate a VMEbus interrupt. Since this signal is always active, there will probably be an interrupt pending associated with it. Therefore, when the Interrupt Control Register is set to enable interrupts for this source, an interrupt would be immediately generated. To clear this pending interrupt, simply read or write the PINTCLR0 register before enabling interrupt source 0 with INTCR0.

3.4.2 INTERRUPT SOURCE 1 (Future Implementation)

3.4.3 INTERRUPT SOURCE 2 (Heartbeat Pulses Not Implemented)

The rate programmable heartbeat pulses can be used to generate VMEbus interrupts. Use INTCR2, INTV2, and PINTCLR2 to control this interrupt source. The interrupt is generated on the rising edge of the heartbeat pulse.

3.4.4 INTERRUPT SOURCE 3 (Time Valid)

Interrupt Source 3 is used to inform the user that a valid time (External Event or Time Request) has been loaded into the Time Data Block without having to poll the Time Valid Flag Register. The Data Valid Interrupt Control Register (offset 003) is used (along with INTCR3, INTV3, and PINTCLR3) to enable this interrupt. The user should clear any source 3 pending interrupts before enabling interrupts with INTCR3 by accessing the PINTCLOR3 Register. Also, be sure to read the INT3ACK register after servicing the interrupt or subsequent interrupt cannot take place.

CHAPTER FOUR
I/O CONNECTIONS

4.0 J1 SIGNAL I/O CONNECTOR (9 PIN DS)

Pinout assignments for this connector are shown in Table 4-1. Pin assignments for the P2 connector are also shown in Table 4-1.

4.1 J2 TIMECODE OUTPUT (BNC)

Time code output modulated sine wave, or DC level shift selected via JP7 and JP2.

4.2 J3 TIMECODE INPUT

The timecode input is available on the front panel BNC labeled 'J3' and is connected in parallel with the other connectors which carry this signal.

4.3 J4 AND J5 RS-422 PHONE JACK I/O

These connectors are for diagnostic use only. See schematic diagram 11420-A for pin assignments. An IBM PC or compatible may use J4 by connecting ground to J4-2 or J4-5 and RX in to J4-4.

Table 4-1
Bc350VME J1/P2 I/O Pinouts

J1	P2	Signal Description
1	C16	Analog Input #2 (not used)
2	C14	Analog Input #1 (not used)
3	C6	Event Input
4	C9	Heartbeat Output (not used)
5	C8	Heartbeat Output (not used)
6	C12	10 MHz Output (disciplined)
7	C11	1 PPS Output (disciplined)
8	A1-A17	Ground
9	A19	Ground
-	C1	Time Code Input
-	C2	Time Code Return
-	C4	Time Code Output (Generator)
-	C7	Time Code 1PPS Output
-	C10	External 1PPS Input

CHAPTER FIVE
THEORY OF OPERATION

5.0 GENERAL

This chapter explains the theory of operation for the bc350VME.

5.1 THEORY OF OPERATION

The bc350VME circuitry consists of the VMEbus interface, the dual port SRAM (control and data registers), the IRIG B reader MPU, the generator MPU, and the display.

The VMEbus interface allows the control and data registers (dual port SRAM U22) to be written and read. The VMEbus interface is similar to the bcTDM interface.

The IRIG B reader MPU consists of a Motorola 68HC11 MPU (U16), a firmware EPROM (U14), a RAM (U8), and an address decoder PLD (U18). The time code signal is routed to PLL U13 which phase locks to the IRIG B carrier and generates a quadrature clock (pin 16). When this clock transitions from low to high, the MPU performs an A/D conversion on the time code signal. This digital data is analyzed by the MPU to decode the IRIG B time code data. The MPU generates a 1PPS signal (U16-28) which is used to synchronize the IRIG B and CDG generators to the range time.

The IRIG B reader MPU also disciplines a 10 MHz VCXO in order to synchronize it to the incoming IRIG B timecode. The control input to the VCXO is generated by the 82C54 counter-timer chip which generates a variable pulse width signal which is low pass filtered by R10 and C21 to produce a DC level between 0V and 5V. The 10 MHz clock drives the U27 Logic Cell Array (LCA) which contains a 7 decade BCD counter chain inside. The output of this counter chain drives a digital sine wave generator which is used to develop the analog time code signal. This sine wave generator consists of the U21 EPROM which holds the digital sine waves data, the U31 D/A converter, and the U2 U3 amplifier, driver.

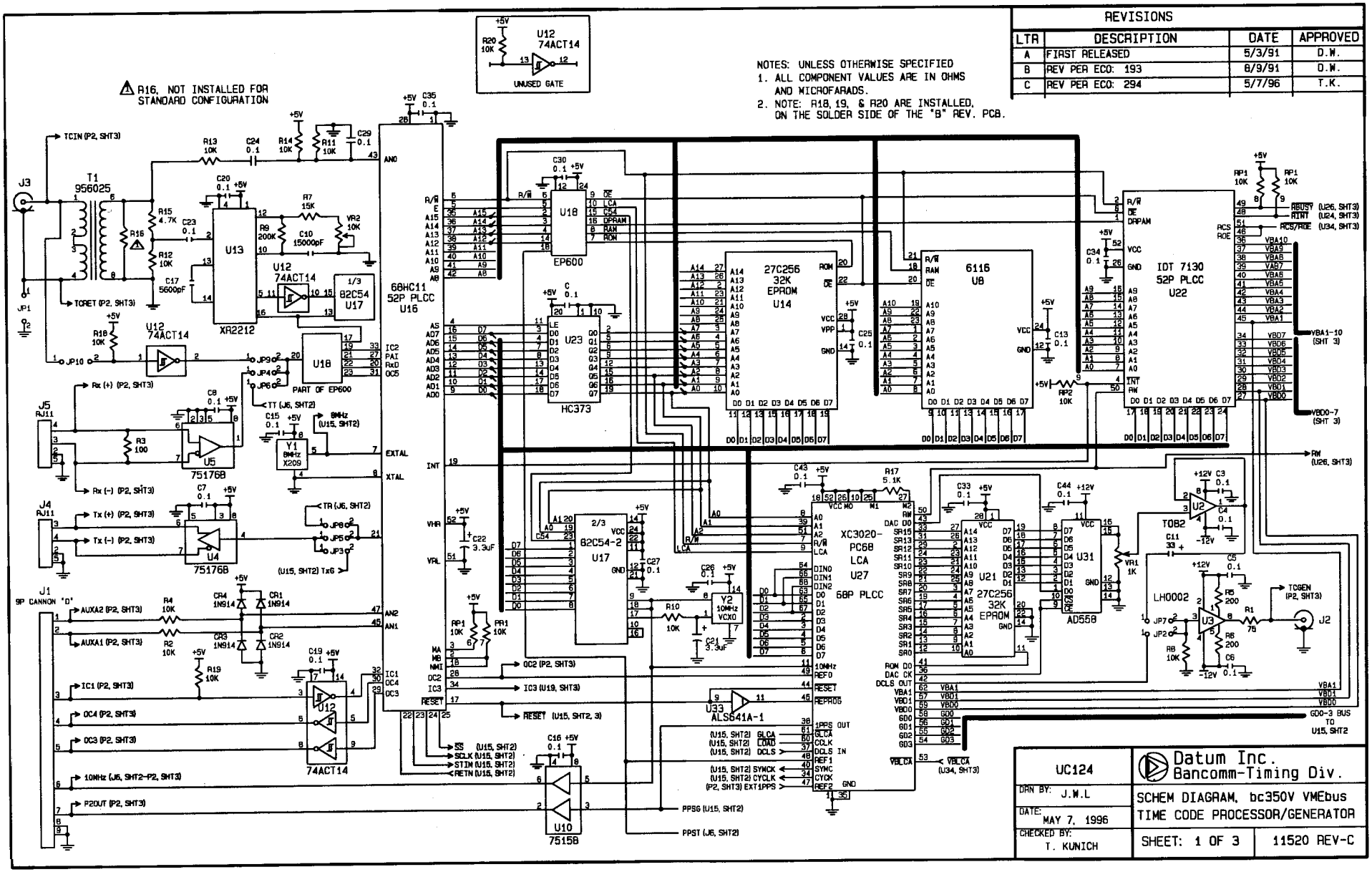
The generator MPU consists of a Motorola 68HC11 MPU (U15), a firmware EPROM (U6), a RAM (U9) and an address decoder PLD (U11). The IRIG B MPU sends the generated time data to the generator MPU via the 68HC11 synchronous serial interface. The generator MPU controls the sine wave amplitude by providing a DC level shift signal to the LCA (U27-37). The DC level shift signal is relocked inside the LCA to become synchronous with the counter chain.

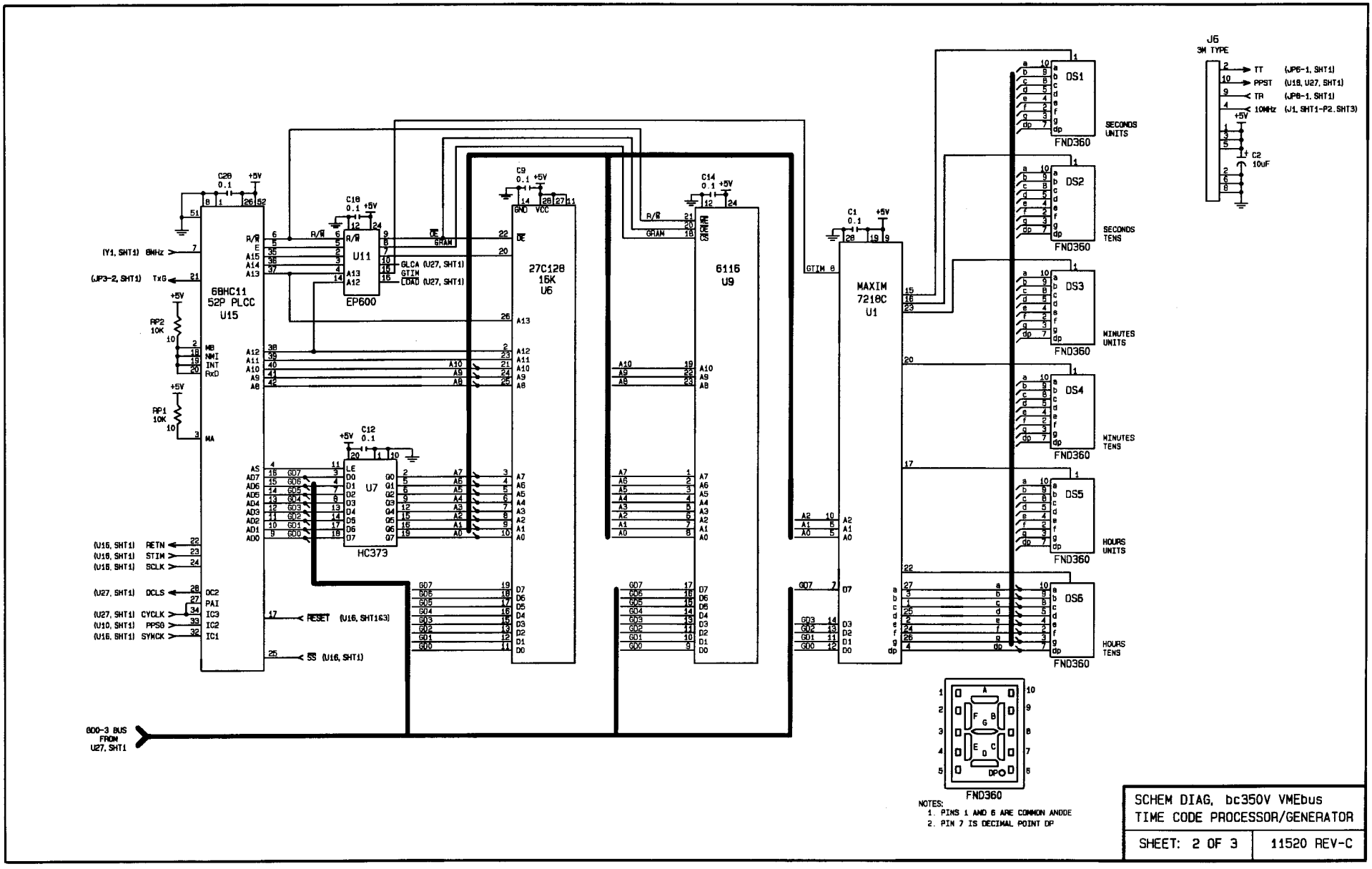
The generator MPU also controls the front panel display. The display controller IC (U1) takes care of multiplexing the 6 digit display and driving the LED digits. The MPU simply loads U1 with the time to be displayed.

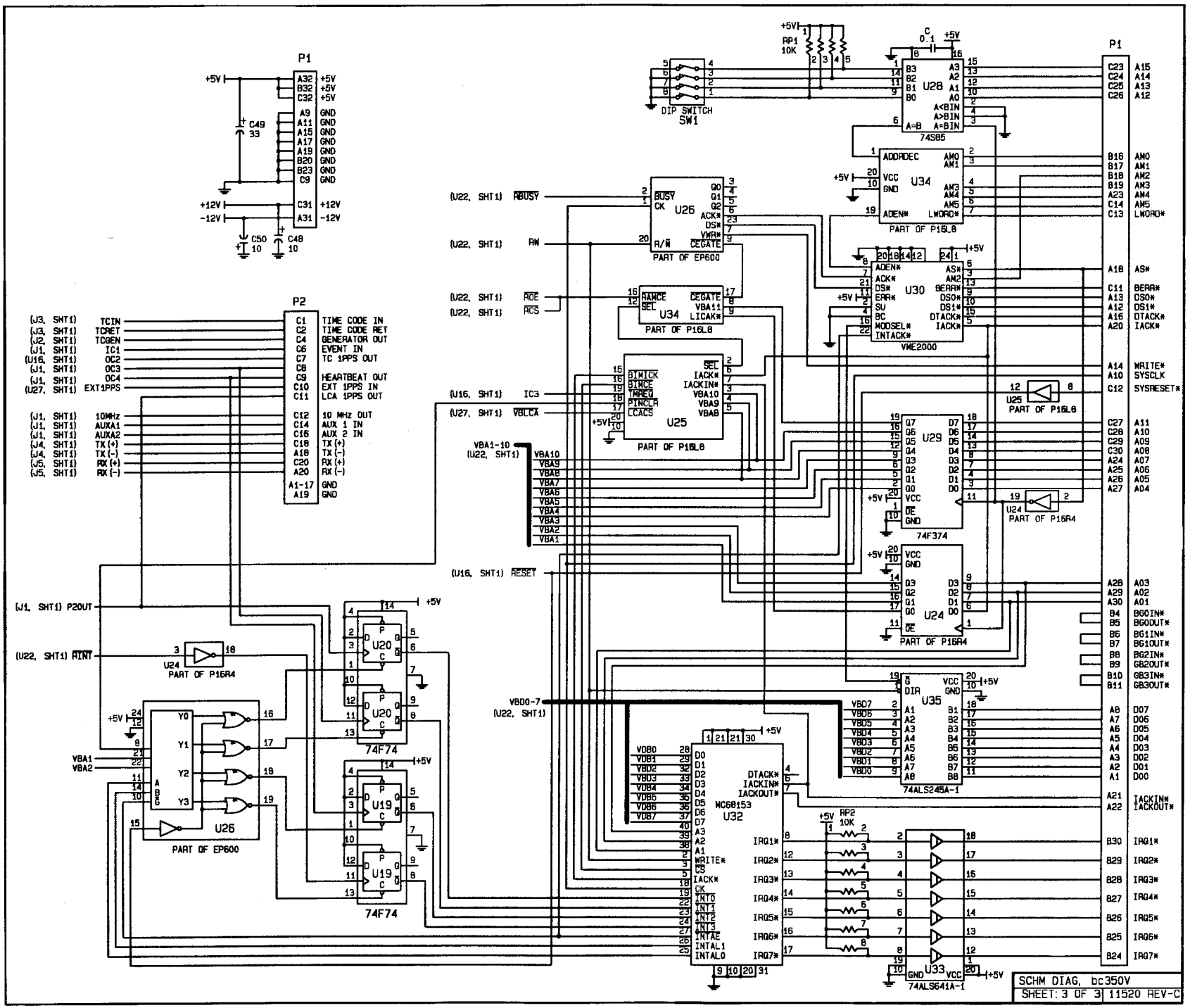
CHAPTER SIX
DRAWING SET

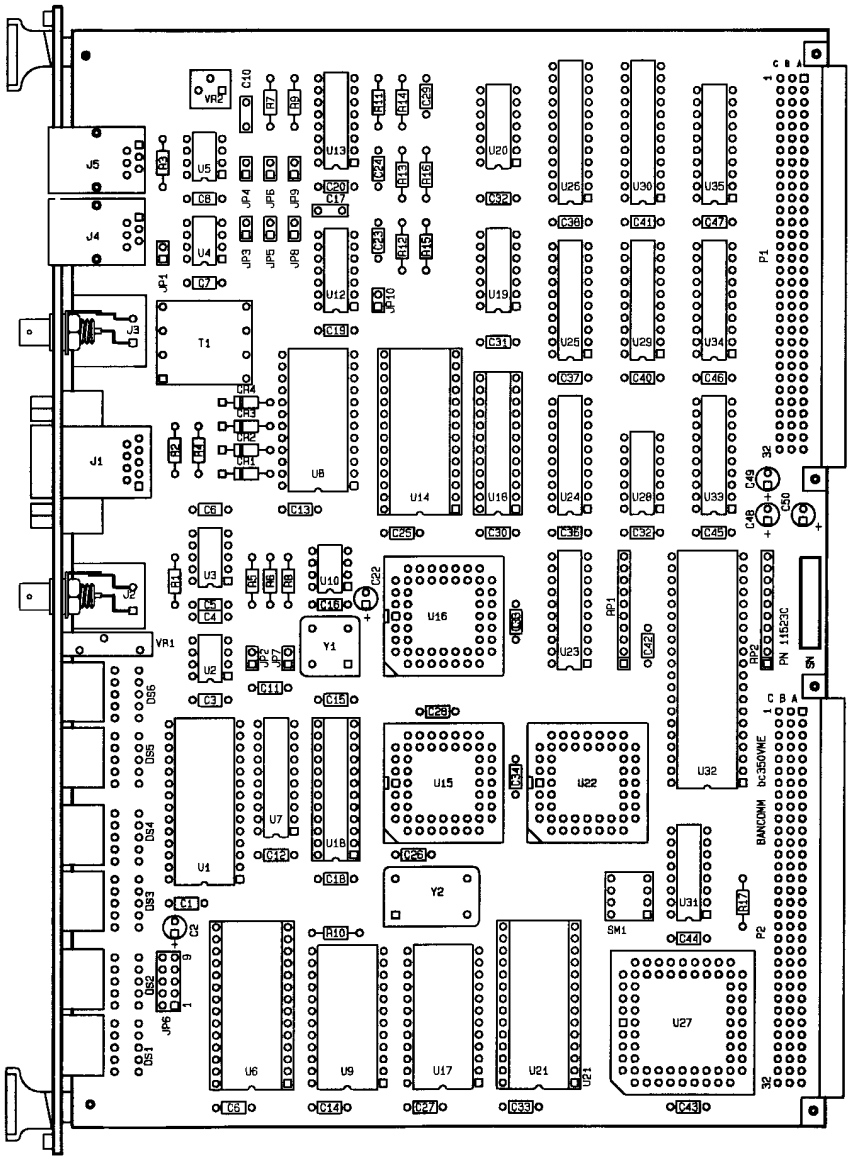
6.0 GENERAL

This chapter contains the schematic diagram, assembly drawing, and parts list for the bc350VME.

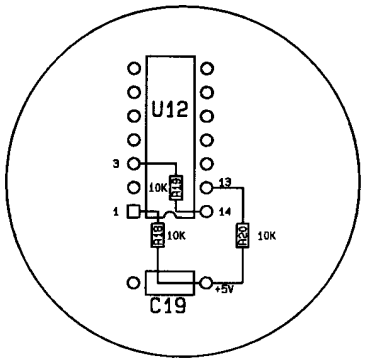

REVISIONS
LTR | DESCRIPTION | DATE | APPROVED
A | FIRST RELEASED | 5/3/91 | D.W.
B | REV PER ECO: 193 | 8/9/91 | D.W.
C | REV PER ECO: 294 | 5/7/96 | T.K.
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL COMPONENT VALUES ARE IN OHMS AND MICROFARADS.
2. NOTE: R18, 19, & R20 ARE INSTALLED, ON THE SOLDER SIDE OF THE "B" REV. PCB.
R16, NOT INSTALLED FOR STANDARD CONFIGURATION
UNUSED GATE
68HC11 52P PLCC U16
EP600
27C256 32K EPROM U14
6116 U8
IDT 7130 52P PLCC U22
HC373
82C54-2 U17
XC3020-PC68 LCA U27
68P PLCC
27C256 32K EPROM U21
AD558
ALS641A-1
74ACT14
751768
75158
XR2212
LH0002
T082
UC124
Datum Inc. Bancomm-Timing Div.
SCHEM DIAGRAM, bc350V VMEbus TIME CODE PROCESSOR/GENERATOR
DRN BY: J.W.L
DATE: MAY 7, 1996
CHECKED BY: T. KUNICH
SHEET: 1 OF 3
11520 REV-C


J6
3M TYPE
TT (JP6-1, SHT1)
PPST (U18, U27, SHT1)
TR (JP8-1, SHT1)
10MHz (J1, SHT1-P2, SHT3)
C2 10uF
6BHC11 52P PLCC U15
EP600
U11
27C128 16K U6
6116 U9
HC373
U7
MAXIM 7218C U1
DS1
DS2
DS3
DS4
DS5
DS6
FND360
SECONDS UNITS
SECONDS TENS
MINUTES UNITS
MINUTES TENS
HOURS UNITS
HOURS TENS
(Y1, SHT1) 8MHz
(JP3-2, SHT1) TxG
(U16, SHT1) RETN
(U16, SHT1) STIM
(U16, SHT1) SCLK
(U27, SHT1) DCLS
(U27, SHT1) CYCLK
(U10, SHT1) PPS0
(U16, SHT1) SYNCK
RESET (U16, SHT1&3)
SS (U16, SHT1)
GD0-3 BUS FROM U27, SHT1
GTIM 0
NOTES:
1. PINS 1 AND 6 ARE COMMON ANODE
2. PIN 7 IS DECIMAL POINT DP
SCHEM DIAG, bc350V VMEbus
TIME CODE PROCESSOR/GENERATOR
SHEET: 2 OF 3
11520 REV-C


P1
P2
U24
U25
U26
U28
U29
U30
U32
U33
U34
U35
U19
U20
74F74
74S85
74F374
74ALS245A-1
74ALS641A-1
VME2000
DIP SWITCH
SW1
PART OF EP600
PART OF P16L8
PART OF P16R4
SCHM DIAG, bc350V
SHEET: 3 OF 3 11520 REV-C



REVISIONS			
LTR	DESCRIPTION	DATE	APVD
A	FIRST RELEASE	05-03-91	D.W.
B	REV PER ECO# 193	08-09-91	D.W.
C	REV PER ECO# 294	05-07-96	T.K.



MODIFICATION SHOWING RESISTOR POSITIONS
REV-B TO REV-C. SOLDER SIDE SHOWN

UC124 FILE: A350_C1.SCH	Datum Inc Bancomm-Timing Division	
DRAWN BY: JWL	ASSY, bc350VME VMEbus	
DATE: MAY 7, 1996	TIME CODE PROCESSOR/GEN.	
APP. BY: T. KUNICH	SHEET: 1 OF 3	11523-C

Assembly, Parts Listing
bc350VME Time Code Processor/Generator

Ref: Drawing No. 11523 C
Ref: UC 124
May 7, 1996

OPT	BC P/N	MANF P/N	MANUFACTURE	VALUE	DESCRIPTION	QTY#	REF DESIG.
	1503335	335RMR035M	IC	3.3 MF, 35V	ALUMINUM ELECTROLYTIC CAP.	2.00	C21,22
	1503336	336RMR025M	IC	33 MF, 35V	ALUMINUM ELECTROLYTIC CAP.	4.00	C11,48,49,50
	1504106	196D106X9035PE4	SPRAGUE	10 MF, 35V	TANTALUM CAP, RADIAL LEADS	1.00	C2
	1506153	SR211C153KAA	AVX	15000 PF, 100V	MONO CERAMIC CAPACITOR .2 R/L	1.00	C10
	1506562	SR211C562KAA	AVX	5600 PF, 100V	MONO CERAMIC CAPACITOR .2 R/L	1.00	C17
	1515104	MD015E104MAA	AVX/67349	0.1 MF, 50V	DIP GUARD CAPACITOR	41.00	C1,3-9,12-16,18-20,23-47
	1701124	11522-C	BANCOMM DIV, DATUM	bc350V Pros/Gen	PRINTED CIRCUIT BOARD	1.00	PCB1
	2101003	31-221	AMPHENOL	50 OHM	FRONT MNT BNC BULKHEAD RECEP.	1.00	BKT1 J2
	2101004	31-10	AMPHENOL	50 OHM	FRONT MNT ISOLATED BNC RECEPT.	1.00	BKT1 J3
	2104001	913346	ERNI	96 POS	DIN CONNECTOR, MALE	2.00	P1,2
	2111010	3591-6002	3M	10 POS	CONTACT HEADER	1.00	J6
	2117061	TSW-130-07-G-D	SAMTEC	2X30 POS	STRAIGHT TERMINAL STRIP	1.00	JP1-10 (CUT AS REQ)
	2124009	747459-3-4	AMP	09 POS	'D' SOCKET, .59 RTANG PCB MNT	1.00	J1
	2148010	10-2822-90C	ARIES	10 POS	RTANG PCB MOUNT, LED SOCKET	6.00	DS1-6
	2149024	824-AG31D	AUGAT	24 POS	SLIM DIP SOCKET	3.00	U11,18,26
	2150020	10620-01-445	ANDON/SPECIRA	20 POS	DIP SOCKET	2.00	U24,34
	2150028	10628-01-445	ANDON/SPECIRA	28 POS	DIP SOCKET	3.00	U6,14,21
	2152052	641748-2	AMP	52 POS	PLCC REC CHIP CARRIER	3.00	U15,16,22
	2152068	641749-1	AMP	68 POS	PLCC REC CHIP CARRIER	1.00	U27
	2190001	520250-3	AMP	1 PORT, 6 POS	PCB RJ11 RECEPTICAL	2.00	J4,5
	2305002	C0-401V-AX	VECTRON	10 MHz	VCXO	1.00	Y2
	2306008	X209	DIGI-KEY	8MHz	HALF SIZE TTL/CMOS CLOCK OSC	1.00	Y1
	2401608	11525A	BANCOMM DIV, DATUM		bc350V FRONT PANEL	1.00	BKT1
	2404600	VME-6U-1450	PHILLIPS COMPONENTS		VME EXTRACTOR HANDLES KIT	1.00	BKT1
	2802001	3341-1L	3M		JACK SCREW KIT	1.00	BKT1
	3703002	LTS360HR	LITEON	HI-BRIGHT	7 SEGMENT DISPLAY, 0.36 INCH	6.00	REF: DS1-6
	4701101	RC07GF101J	ALLEN BRADLEY	100 OHM, 1/4W	FIXED RESISTOR	1.00	R3
	4701103	RC07GF103J	ALLEN BRADLEY	10 K OHM, 1/4W	FIXED RESISTOR	8.00	R2,4,8,10,12,18-20
	4701104	RC07GF104J	ALLEN BRADLEY	100 K OHM, 1/4W	FIXED RESISTOR	2.00	R11,14
	4701153	RC07GF153J	ALLEN BRADLEY	15 K OHM, 1/4W	FIXED RESISTOR	1.00	R7
	4701201	RC07GF201J	ALLEN BRADLEY	200 OHM, 1/4W	FIXED RESISTOR	2.00	R5,6
	4701204	RC07GF204J	ALLEN BRADLEY	200 K OHM, 1/4W	FIXED RESISTOR	1.00	R9
	4701221	RC07GF221J	ALLEN BRADLEY	220 OHM, 1/4W	FIXED RESISTOR	1.00	R13
	4701472	RC07GF472J	ALLEN BRADLEY	4.7 K OHM, 1/4W	FIXED RESISTOR	1.00	R15
	4701512	RC07GF512J	ALLEN BRADLEY	5.1 K OHM, 1/4W	FIXED RESISTOR	1.00	R17
	4701750	RC07GF750J	ALLEN BRADLEY	75 OHM, 1/4W	FIXED RESISTOR	1.00	R1
	4703103	72P103	BECKMAN	10 K OHM, 1/2W	SINGLE TURN POTENTIOMETER	1.00	VR2
	4704102	89PR1K	BECKMAN	1 K OHM, 1/2W	POTENTIOMETER	1.00	VR1
	4705103	710A103	ALLEN BRADLEY	10 K OHM, 1/8W	C-SIP RESISTORS, 10 PIN 'X'	2.00	RP1,2
	4803001	IN914			SILICON DIODE	4.00	CR1-4
	5108001	76SB04	GRAYHILL		4PST DIP SWITCH	1.00	SW1
	5603002	956025	DATUM INC	08P DIP PKG	TRANSFORMER	1.00	T1
	9002510	74ACT14	RCA	14P DIP PKG	HEX SCHMITT INVERTER	1.00	U12
	9006818	74F74	NATIONAL	14P DIP PKG	DUAL D FLIP FLOP	2.00	U19,20
	9006858	MM74F374N	NATIONAL	20P DIP PKG	OCTAL D FLIP FLOP	1.00	U29
	9008657	74HC373	VARIOUS	20P DIP PKG	OCTAL D TRANSPARENT LATCH, T/S	2.00	U7,23
	9015222	74S85	NATIONAL	16P DIP PKG	4-BIT MAGNITUDE COMPARATOR	1.00	U28
	9102002	68HC11A1FN	MOTOROLA	52P PLCC PKG	MICROCOMPUTER	2.00	U15,16 (SKT)
	9103008	82C54-2	AMD	24P DIP PKG .6W	CMOS COUNTER TIMER	1.00	U17
	9103031	MX68C153	MACRONIX	40P DIP PKG .6W	CMOS BUS INTERRUPT MODULE	1.00	U32
	9203005	AD558JN	ANALOG	16P DIP PKG	8 BIT DACPORT	1.00	U31
	9204020	ICM7218CIPI	MAXIM	28P DIP PKG .6W	8 DIGIT LED DISPLAY DRIVER	1.00	U1
	9207070	SN75158P	TI	08P DIP PKG	DUAL 50 OHM TTL LINE DRIVER	1.00	U10
	9207076	SN75176B	TI	08P DIP PKG	DIFF BUS TRANS	2.00	U4,5
	9207920	SN74ALS245A-1N	TI	20P DIP PKG	OCTAL BUS TRANSCEIVER	1.00	U35
	9207925	SN74ALS641A-1N	TI	20P DIP PKG	OCTAL BUS TRANSCEIVER	1.00	U33
	9211001	VME2000-45	PLX TECHONLOGY	24P DIP	VME SLAVE INTERFACE	1.00	U30
	9306005	LH0002CN	NATIONAL	10P DIP PKG	CURRENT AMPLIFIER	1.00	U3
	9306035	TL082	TI	08P DIP PKG	DUAL BIPOLAR JFET OP AMP	1.00	U2
	9307030	XR2212CP	EXAR	16P DIP PKG	PHASE LOCKED LOOP	1.00	U13
	9405001	EP600DC-3	ALTERA	24P DIP PKG .3W	EPLD	3.00	U11,18,26
	9405015	PAL16L8B	MMI	20P DIP PKG .3W	PAL	2.00	U25,34
	9405020	PAL16R4ACN	MMI	20P DIP PKG .3W	PAL 35 NS	1.00	U24
	9405045	XC3020-50PC68C	XILINX	68P PLCC PKG	PLD	1.00	U27 (SKT)

Ref: Drawing No. 11523 C
Ref: UC 124
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OPT	BC P/N	MANF P/N	MANUFACTURE	VALUE	DESCRIPTION	QTY#	REF DESIG.
	9406040	27C256	VARIOUS	28P DIP PKG .6W	32 K BYTE, CMOS EPROM	2.00	U14,21
	9406308	27C128		28P DIP PKG .6W	16 K BYTE EPROM	1.00	U6
	9407055	IDT6116SA150P	IDT	24P DIP PKG .6W	8 X 2048 CMOS STATIC RAM	2.00	U8,9
	9407660	IDT7130LA70J	IDT	52P PLCC PKG	1K X 8 DUAL PORT RAM	1.00	U22 (SKT)